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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,398	07/10/2002	Donato Forlenza	BUR920010133US1	7444

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IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
1000 RIVER STREET
972 E
ESSEX JUNCTION, VT 05452

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,398	FORLENZA ET AL.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-11 and 15* is/are allowed.

6)☒ Claim(s) *1-6 and 13* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a FINAL Office Action in response to AMENDMENT filed 8/27/2004 responsive to the Prior Office Action, dated 6/30/2004.

Claims 1-15 were previously examined in the Prior Office Action, without applying prior art rejection, because of claim rejections under 35 U.S.C. 112, second paragraph, as being generally indefinite.

Claims 12 and 14 are cancelled. Claims 1-11, 13 and 15 are pending and under examination.

Objection to the specification is withdrawn, in view of the proper required number of words.

Objection to the claims because of various informalities is withdrawn in response to correction to the claims, as required by the prior Office Action.

Claims rejection under 35 U.S.C. 112, second paragraph, is withdrawn in response to the amendment to the claims, as required by the prior Office Action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lindberg et al. (US PATENT NO: 5,663,967, ISSUED: September 2, 1997).

Regarding independent Claim 1, Lindberg discloses a method for the isolation of defects in multi-level, high-density, application-specific, integrated circuit semiconductor device, comprising:

Selecting semiconductor device (44) under test, having logic circuits formed of latches, wherein the device comprises primarily combinational logic 22 and a number of latches or flip-flops 24, 26, and 28, as well as the various inputs, control lines, and a clock input, Figures 1 and 7.

Testing the logic circuits in the device, as follows: "when the chip is being tested, scan enable 30 is asserted, and data is clocked serially into the latches (which form a shift register) via a scan input pin (ti). To test the scan latches, patterns of 1's and 0's can be shifted in through the scan chain at the scan input pin (ti) to the scan output. To test the combinational portion of the circuit, the scan enable pin (te) is enabled and a test pattern is shifted serially into the latches.

Locating a failing logic circuit in the device by performing the scan integrity check, where a scan pattern of alternating 1's and 0's is simply shifted through the scan chain, with no system clock applied. The data at the Scan out pin is compared with the scan input data. If any fault is detected, then the process continues with step 120 to identify the failing location, wherein a binary search is conducted using an electron beam probe.

Combining a functional test procedure and the structural design technique to dynamically crate a new test pattern based on the local failure, as shown in Figures 2 and 2A, as follows: Step 114 (Figure 2A) determines whether the suspect fault locations have been localized with sufficient particularity. If the suspect fault list is large, then a new set of is patterns are generated in step 116 and the whole procedure from testing in step 118 to mapped simulation scan patterns in step 104 to fault localization in steps 108, 110, and 112 is repeated. The new scan patterns serve as the verification patterns necessary to further localize and verify the defects indicated by the faults in the suspect fault list.

Diagnosing the failing circuit, step 120, such as a failure location, (f1 or f2), wherein fault (f1) is an example of a fault occurring in the combinational portion of the scan-path, and (fault f2) is an example of a fault occurring directly in the scan-path. The location and the type of fault can be identified from the list of suspect faults using a diagnostic tool such as an electron beam probe, and the type of fault is "stuck-at-1" or "stuck-at-0".

Regarding Claims 2, 13, Lindberg discloses the step of combining of claim 1, including transforming a functional pattern (1's and 0's) generated by the pattern generator 48 into a scan deterministic pattern, such as a serial pattern of 1's and 0's, which is shifted through the scan chain (flip-flops 24, 26, 28) at the scan input pin (ti) to the scan output, Figure 1.

Regarding Claims 3-6, Lindberg discloses wherein the failed logic circuit is diagnosed as having type of fault "stuck-at-1" or "stuck-at-0", and functional faults.

Allowable Subject Matter

3. Claims 7-11 and 15 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention, including the claimed features, recited, inter alia, as follows:

Independent claim 7, recites, inter alia, the claimed features of unloading the values of all the latches from the scan chain before the identified failing latch, generating a load from the unloaded values of all the latches from the scan chain before the identified failing latch, applying the generated Load as the first event of an LSSD deterministic pattern by using the same identical primary inputs and clocks that produced the failure in the failing latch in the first semiconductor device to the second semiconductor correctly operating device using a bootstrap technique.

Similarly, independent claim 10 recites, inter alia, the claimed features of observing the states of the logic circuit containing the failed latch by unloading the values of the plurality of latches from the LSSD scan chain positioned in the scan chain before the identified failing latch which includes reading any embedded circuit memories and other circuit storage elements positioned in the scan chain before the identified failing latch, generating a load from the unloaded states of the latches positioned in the scan chain before the failed latch, applying the generated Load as the first event of a newly created independent LSSD deterministic pattern by using the primary inputs and

clock signals identical to the primary inputs and clock signals that produced the failure to a known correctly operating device utilizing logic circuits formed of a plurality of lathes arranged in LSSD scan chain and a plurality of other circuit storage elements identical to the failed device by applying a plurality of primary inputs and clock signals to the device by using a bootstrap technique.

Consequently, independent claims 7 and 10 are allowed over the prior arts of record. Claims 8, 9 and 15 are directly or indirectly depended upon claim 7, and therefore are allowable, and claim 11 is depended upon claim 10, and therefore is also allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

4. Applicant's arguments with respect to claims 1-11, 13 and 15 have been considered but are moot in view of the new grounds of rejection. Claims 1-6 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lindberg et al. (US PATENT NO: 5,663,967), and Claims 7-11 and 15 are allowed, as set forth in the present Office Action.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Randolph Building
401 Dulany Street,
Alexandria, VA 22314
Tel (571) 272-3824, Fax (571) 273-3824
Email: james.kerveros@uspto.gov

Date: 6 April 2005
Office Action: Final Rejection

By: _____.

JAMES C KERVEROS
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100